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10/754,483	01/09/2004	Kevin Conley	SDK1P017/503	6185

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EXAMINER	
CAMPOS, YAIMA	

ART UNIT	PAPER NUMBER
2185	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USPTOmail@beyerlaw.com

Office Action Summary	Application No.	Applicant(s)	
	10/754,483	CONLEY ET AL.	
	Examiner	Art Unit	
	YAIMA CAMPOS	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *39-55 and 57-62* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *39-55, 57-62* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. As per the instant Application having Application number 10/754,483, the examiner acknowledges the applicant's submission of the amendment dated 12/29/2009. At this point, claims 39, 43-45, 49-51, 57 and 61-62 have been amended, and claims 1-38 and 56 have been canceled. Claims 39-55 and 57-62 are pending.

REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 8 recites the limitation "the order used under the second scheme " in line 2. There is insufficient antecedent basis for this limitation in the claim. The applicants might consider amending this claim to read –**an order used under the second scheme**–.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 39-55 and 57-62** are rejected under 35 U.S.C. 103(a) as being unpatentable over Suda (US 2004/0123059) in view of Moro (US 2004/0107316).

6. As per claim 39. A method for reading data from a memory card that provides non-volatile data storage having an address space defined by a contiguous range of addresses, the method comprising: determining whether a mechanical switch on the memory card is in a first, second, or third position; **["mechanical switches 16a and 16b for selecting one of the plural storage areas… when the mechanical switches… are set to positions marked as "1," the controller 10 reflects the state of the switches... thereby allowing a memory card host device to handle the first storage area… when… set to position marked as "2"… thereby allowing the memory card host device to handle the second storage area… it is acceptable if the memory card 3 includes plural internal registers 12a, 12b, 12c, and 12d for the respective plural storage areas as shown in FIG. 1... it is also acceptable that the memory card 3 includes the internal register 18 for the plural storage areas as shown in FIG. 3" (par. 0069; fig. 7 and related text); *thus determining the position of a switch*]**
when the mechanical switch is in a first position: accessing a first partition of the address space using a first file system; when the mechanical switch is a second position: accessing a second partition of the address space using the first file system; and when the mechanical switch is in a third position: accessing a third partition of the address space using a second file system **[Suda discloses "when the mechanical switches… are set to positions marked as "1," the controller 10 reflects the state of the switches... thereby allowing a memory card host device to handle the first storage area… when… set to position marked as "2"… thereby allowing the memory card host device to handle the second storage area… it is acceptable if the**

memory card 3 includes plural internal registers 12a, 12b, 12c, and 12d for the respective plural storage areas as shown in FIG. 1... it is also acceptable that the memory card 3 includes the internal register 18 for the plural storage areas as shown in FIG. 3… it is acceptable if the memory card 3 includes plural internal registers 12a, 12b, 12c, and 12d for the respective plural storage areas as shown in FIG. 1... it is also acceptable that the memory card 3 includes the internal register 18 for the plural storage areas as shown in FIG. 3" (par. 0069; fig. 7 and related text); ***thus determining which of a plurality of volumes to access based on a the position of a switch.*** **Suda further discloses "when a FAT 16 is used as the file system, the marginal capacity is equal to 2 gigabytes… the marginal capacity of the entire memory card is equivalent to 8 gigabytes when the memory card includes four storage areas" (par. 0028);** ***thus disclosing a memory card comprising plural storage areas which utilize a FAT 16 file system*** **and also teaches an embodiment in which the memory comprising multiple storage areas may use a first file system such as file system A in a first storage and a second file system, such as file system B in a second storage area (fig. 6 and relate text; pars. 0063-0064) wherein fig. 6 discusses two storage areas, each having a different file system, however, Suda explains that the memory card according to fig. 6 "includes two or more storage areas" (par. 0063)]**; however, Suda does not expressly disclose the third storage area in the embodiment of figs. 1 and 7 using a second file system.

Moro discloses a memory card comprising a plurality of partitions, wherein a partition uses a first file system and another partition uses a second file system as **[memory card 32 comprising a first partition using FAT 16 file system and second partition using FAT 32 file system (fig. 1 and related text; par. 0028) and explains "the memory card 32 may include**

more than two partitions. In such case, information on each of the partitions will be saved in the master boot sector 161" (par. 0051; fig. 6 and related text)].

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the memory card which comprises multiple volumes or partitions which are accessed based on the position of a mechanical switch, wherein each of the plurality of storage areas may use a different file system, as described by Suda, and more specifically configure the third storage area as taught by Suda to use a second file system in the manner that Moro teaches a memory card wherein partitions of the memory card may use different file systems since doing so would allow the memory card of Suda to **[be able to increase the capacity of a memory and facilitate user access (pars. 0007 and 0038)]**.

Therefore, it would have been obvious to combine Suda with Moro for the benefit of creating a method for reading data from a memory card to obtain the invention as specified in claim 39.

7. As per claim 40. The method of claim 39, wherein the first file system utilizes 16 bit addressing and the second file system utilizes greater than 16 bit addressing **[Suda teaches memory card having plural area where each may utilizing a FAT 16 file system (par. 0028). Moro teaches the second file system utilizes FAT 32 addressing (par. 0028)]**.

8. As per claim 41. The method of claim 39, wherein the first file system is the FAT-16 file system **[Suda teaches memory card having plural area where each may utilizing a FAT 16 file system (par. 0028). Moro teaches the second file system utilizes FAT 32 addressing (par. 0028)]**.

9. As per claim 42. The method of claim 39, wherein the second file system is the FAT-32 file system **[Moro teaches the second file system utilizes FAT 32 addressing (par. 0028)]**.

10. As per claim 43. The method of claim 40, wherein each of the first and second partitions has a maximum size of 2GB **[Suda teaches "when a FAT 16 is used as the file system, the marginal capacity is equal to 2 gigabytes… the marginal capacity of the entire memory card is equivalent to 8 gigabytes when the memory card includes four storage areas" (par. 0028); *therefore, each FAT 16 or 16-bit file system storage area having a maximum size of 2 Gbytes*]**.

11. As per claim 44. The method of claim 39, wherein the first file system is determined by reading an address space uniquely associated with either the first or second partitions and the second file system is determined by reading an address space uniquely associated with the third partition **[Suda discloses one embodiment comprising each of memory areas managed by a single file system (par. 0028) and another embodiment in which each storage area of memory card uses a different file system (par. 0063; fig. 6 and related text) and Moro discloses first partition information including FAT 16 and second partition information including FAT 32 information wherein that the FAT 16 partition information is stored in an address/space or range uniquely associated with the first partition and the FAT 32 partition information is stored in an address space/range uniquely associated with the second partition (fig. 1 and related text; par. 0028)]**.

12. As per claim 45. A memory card comprising: non-volatile data storage that provides data storage having an address space with three partitions; **[Suda discloses memory card 3 which comprises a plurality of storage areas (figs. 1, 6 and 7 and related text)]**

a switch being set in one of a plurality of switch positions; and **["mechanical switches 16a and 16b for selecting one of the plural storage areas… when the mechanical switches… are set to positions marked as "1," the controller 10 reflects the state of the switches... thereby allowing a memory card host device to handle the first storage area… when… set to position marked as "2"… thereby allowing the memory card host device to handle the second storage area… it is acceptable if the memory card 3 includes plural internal registers 12a, 12b, 12c, and 12d for the respective plural storage areas as shown in FIG. 1... it is also acceptable that the memory card 3 includes the internal register 18 for the plural storage areas as shown in FIG. 3" (par. 0069; fig. 7 and related text);** ***thus determining the position of a switch***]

a controller that manages access to the data stored in said non-volatile storage, **[Suda discloses controller 10 (figs. 1, 6 and 7 and related text)]**

wherein the controller is configured to determine whether the switch is in a first, second or third position and when the switch is in a first position: access a first partition of the address space using a first file system; when the switch is in a second position: access a second partition of the address space using the first file system; and when the switch is in a third position: access a third partition of the address space using a second file system **[Suda discloses "when the mechanical switches… are set to positions marked as "1," the controller 10 reflects the state of the switches... thereby allowing a memory card host device to handle the first storage area… when… set to position marked as "2"… thereby allowing the memory card host device to handle the second storage area… it is acceptable if the memory card 3 includes plural internal registers 12a, 12b, 12c, and 12d for the respective plural storage areas as shown in**

FIG. 1... it is also acceptable that the memory card 3 includes the internal register 18 for the plural storage areas as shown in FIG. 3… it is acceptable if the memory card 3 includes plural internal registers 12a, 12b, 12c, and 12d for the respective plural storage areas as shown in FIG. 1... it is also acceptable that the memory card 3 includes the internal register 18 for the plural storage areas as shown in FIG. 3" (par. 0069; fig. 7 and related text); ***thus determining which of a plurality of volumes to access based on a the position of a switch.*** **Suda further discloses "when a FAT 16 is used as the file system, the marginal capacity is equal to 2 gigabytes… the marginal capacity of the entire memory card is equivalent to 8 gigabytes when the memory card includes four storage areas" (par. 0028);** ***thus disclosing a memory card comprising plural storage areas which utilize a FAT 16 file system*** **and also teaches an embodiment in which the memory comprising multiple storage areas may use a first file system such as file system A in a first storage and a second file system, such as file system B in a second storage area (fig. 6 and relate text; pars. 0063-0064) wherein fig. 6 discusses two storage areas, each having a different file system, however, Suda explains that the memory card according to fig. 6 "includes two or more storage areas" (par. 0063)];** however, Suda does not expressly disclose the third storage area in the embodiment of figs. 1 and 7 using a second file system.

Moro discloses a memory card comprising a plurality of partitions, wherein a partition uses a first file system and another partition uses a second file system as **[memory card 32 comprising a first partition using FAT 16 file system and second partition using FAT 32 file system (fig. 1 and related text; par. 0028) and explains "the memory card 32 may include**

more than two partitions. In such case, information on each of the partitions will be saved in the master boot sector 161" (par. 0051; fig. 6 and related text)].

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the memory card which comprises multiple volumes or partitions which are accessed based on the position of a mechanical switch, wherein each of the plurality of storage areas may use a different file system, as described by Suda, and more specifically configure the third storage area as taught by Suda to use a second file system in the manner that Moro teaches a memory card wherein partitions of the memory card may use different file systems since doing so would allow the memory card of Suda to **[be able to increase the capacity of a memory and facilitate user access (pars. 0007 and 0038)]**.

Therefore, it would have been obvious to combine Suda with Moro for the benefit of creating a memory card to obtain the invention as specified in claim 45.

13. As per claim 46. The memory card of claim 45, wherein the first file system utilizes 16 bit addressing and the second file system utilizes greater than 16 bit addressing **[The rationale in the rejection to claim 40 is herein incorporated]**.

14. As per claim 47. The memory card of claim 45, wherein the first file system is the FAT-16 file system **[The rationale in the rejection to claim 41 is herein incorporated]**.

15. As per claim 48. The memory card of claim 45, wherein the second file system is the FAT- 32 file system **[The rationale in the rejection to claim 42 is herein incorporated]**.

16. As per claim 49. The memory card of claim 46, wherein each of the first and second partitions has a maximum size of 2GB **[The rationale in the rejection to claim 43 is herein incorporated]**.

17. As per claim 50. The memory card of claim 45, wherein the first file system is determined by reading an address space uniquely associated with either the first or second partitions and the second file system is determined by reading an address space uniquely associated with the third partition **[The rationale in the rejection to claim 44 is herein incorporated]**.

18. As per claim 51. An apparatus for reading data from a memory card that provides non-volatile data storage having an address space defined by a contiguous range of addresses, the apparatus comprising: means for determining whether a mechanical switch on the memory card is in a first, second, or third position; means for, when the mechanical switch is in a first position: accessing a first partition of the address space using a first file system; means for, when the mechanical switch is in a second position: accessing a second partition of the address space using the first file system; and means for, when the mechanical switch is in a third position: accessing a third partition of the address space using a second file system. **[The subject matter of claim 51 is parallel to the subject matter of claim 39, except that it sets forth the claimed invention as an apparatus, and it is therefore rejected under the rationale in the rejection to claim 39 above. Claim 51 further requires means for determining** ***(Identified in Applicant's Specification as "host controller" as "The memory card evaluation process 300 is, for example performed by a host controller within memory card" (pages 7-8, pars. 0037 and 0040; fig. 3); taught by the combination Suda and Moro as Suda discloses controller 10 (figs. 1, 6, 7 and related text)),*** **means for accessing** ***(Identified in Applicant's Specification "controller 402" operating memory card for host access (fig. 4; pages 8-9, pars. 0042-0046);***

taught by the combination of Suda and Moro as Suda discloses controller 10 (figs. 1, 6, 7 and related text))].

19. As per claim 52. The apparatus of claim 51, wherein the first file system utilizes 16 bit addressing and the second file system utilizes greater than 16 bit addressing **[The rationale in the rejection to claim 40 is herein incorporated]**.

20. As per claim 53. The apparatus of claim 51, wherein the first file system is the FAT-16 file system **[The rationale in the rejection to claim 41 is herein incorporated]**.

21. As per claim 54. The apparatus of claim 51, wherein the second file system is the FAT-32 file system **[The rationale in the rejection to claim 42 is herein incorporated]**.

22. As per claim 55. The apparatus of claim 52, wherein each of the plurality of volumes has a maximum size of 2GB **[The rationale in the rejection to claim 43 is herein incorporated]**.

23. As per claim 56. The apparatus of claim 51, wherein the means for determining includes means for accessing a portion of the non-volatile data storage stating which file system is utilized **[The rationale in the rejection to claim 44 is herein incorporated]**.

24. As per claim 57. A program storage device readable by a machine, tangibly embodying a set of computer instructions executable by the machine for reading data from a memory card that provides non-volatile data storage having an address space defined by a contiguous range of addresses, the method comprising: determining whether a mechanical switch on the memory card is in a first, second or third position; the non volatile data storage utilizes a first file system or a second file system; when the mechanical switch is in a first position: accessing a first partition of the address space using a first file system, when the mechanical

switch is in a second position: accessing a second partition of the address space using the first file system; and when the mechanical switch is in a third position: accessing a third partition of the address space using a second file system **[The subject matter of claim 57 is parallel to the subject matter of claim 39, except that it sets forth the claimed invention as a program storage device embodying a set of instructions, and it is therefore rejected under the rationale in the rejection to claim 39 above]**.

25. As per claim 58. The program storage device of claim 57, wherein the first file system utilizes 16 bit addressing and the second file system utilizes greater than 16 bit addressing **[The rationale in the rejection to claim 40 is herein incorporated]**.

26. As per claim 59. The program storage device of claim 57, wherein the first file system is the FAT-16 file system **[The rationale in the rejection to claim 41 is herein incorporated]**.

27. As per claim 60. The program storage device of claim 57, wherein the second file system is the FAT-32 file system **[The rationale in the rejection to claim 42 is herein incorporated]**.

28. As per claim 61. The program storage device of claim 58, wherein each of the first and second partitions has a maximum size of 2GB **[The rationale in the rejection to claim 43 is herein incorporated]**.

29. As per claim 62. The program storage device of claim 57, wherein the first file system is determined by reading an address space uniquely associated with either the first or second partitions and the second file system is determined by reading an address space uniquely associated with the third partition **[The rationale in the rejection to claim 44 is herein incorporated]**.

ACKNOWLEDGMENT OF ISSUES RAISED BY THE APPLICANT

Response to Amendment

30. Applicant's arguments filed on 12/29/2009 with respect to claims have been fully considered but are moot in view of the new ground(s) of rejection.

31. However, Applicant's Arguments regarding Suda are not deemed persuasive. As required by **M.P.E.P. § 707.07(f)**, a response to these arguments appears below.

ARGUMENTS CONCERNING PRIOR ART REJECTIONS

32. Claims must be given the broadest reasonable interpretation during examination and limitations appearing in the specification but not recited in the claim are not read into the claim (See M.P.E.P. 2111 [R-1]).

33. Applicant argues "Suda teaches a physical switch being used to select between volumes, but all the volumes are of the same file system. Indeed, none of the prior art teach or suggest having multiple partitions stored using multiple file systems on a single memory card."

In response, these arguments have been fully considered, but are not deemed persuasive since in an embodiment of Suda disclosed regarding fig. 6 and related text, Suda clearly teaches **[a memory card 3 having plural storage areas stored using multiple file systems such as the depicted file system A in first storage area and file system B in second storage area (fig. 6 and related text; pars. 0063-0066)]**.

34. Regarding all other Claims not specifically traversed above and whose rejections were upheld, the Applicant contends that the listed claims are allowable by virtue of their dependence

on other allowable claims. As this dependence is the sole rationale put forth for the allowability of said dependent claims, the Applicant is directed to the Examiner's remarks above. Additionally, any other arguments the Applicant made that were not specifically addressed in this Office Action appeared to directly rely on an argument presented elsewhere in the Applicant's response that was traversed, rendered moot or found persuasive above.

35. All arguments by the applicant are believed to be covered in the body of the office action; thus, this action constitutes a complete response to the issues raised in the remarks dated 12/29/2009.

CLOSING COMMENTS

36. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Examiner's Note

37. Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant, in preparing the responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner.

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

38. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

39. Per the instant office action, claims 39-55 and 57-62 have received an action on the merits and are subject to a final rejection.

b. DIRECTION OF FUTURE CORRESPONDENCES

40. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yaima Campos whose telephone number is (571) 272-1232. The examiner can normally be reached on Monday to Friday 8:30 AM to 5:00 PM.

41. If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Sanjiv Shah, can be reached at the following telephone number: Area Code (571) 272-4098.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

March 22, 2010

/Yaima Campos/
Examiner, Art Unit 2185

/Sanjiv Shah/

Supervisory Patent Examiner, Art Unit 2185